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of

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Application Number

10/630.537

Filing Date

July 29, 2003

First Named Inventor

Sandeep BHATIA

Art Unit

2138

Examiner Name

Phung M. CHUNG

Attorney Docket Number

CA7034222001

[illegible][illegible]

**Examiner
Signature**

/Phung Chung/

Date Considered

01/17/2007

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STATEMENT BY APPLICANT**

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Sheet 2 of 2

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Application Number	10/630,537
Filing Date	July 29, 2003
First Named Inventor	Sandeep BHATIA
Art Unit	2138
Examiner Name	Phung M. CHUNG
Attorney Docket Number	CA7034222001

NON PATENT LITERATURE DOCUMENTS

Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
PC	1	BALAKRISHNAN, K. J., et al., "Deterministic Test Vector Decompression in Software Using Linear Operations", Proceedings of the 21st IEEE VLSI Test Symposium, April 27 - May 1, 2003, pp. 225 - 231, IEEE, Los Alamitos, CA, USA.	
PC	2	BARDELL, P. H. et al., "Build-In Test for VLSI: Pseudorandom Techniques", 1987, pp. 61-313, John Wiley and Sons, New York, USA.	
PC	3	BHATIA, S., "Test Compaction by Using Linear-Matrix Driven Scan Chains", Proceedings of the 18 th IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems, November 3 - 5, 2003, pp. 185 - 190, IEEE, USA.	
PC	4	BHATIA, S., "Test Compaction in a Parallel Access Scan Environment", Proceedings of the 6 th Asian Test Symposium (ATS '97), November 17 - 19, 1997, pp. 300 -305, IEEE, Los Alamitos, CA, USA.	
PC	5	HELLEBRAND, S., et al., "Generation of Vector Patterns Through Reseeding of Multiple-Polynomial Linear Feedback Shift Registers", Proceedings of the International Test Conference, 1992, pp. 120 -124, France.	
PC	6	HSU, F. F. et al., "A Case Study on the Implementation of the Illinois Scan Architecture", Proceedings of the International Test Conference; 2001, pp. 538 - 547, International Test Conference, Washington, D.C., USA.	
PC	7	JARAMILLO, K. et al., "10 Tips for Successful Scan Design: Part One", February 17, 2000, endmag.com, pp. 67 - 73, 75; USA.	
PC	8	JARAMILLO, K. et al., "10 Tips for Successful Scan Design: Part Two", February 17, 2000, endmag.com, pp. 77, 78, 80, 82, 84, 86, 88, 90; USA.	
PC	9	KIEFER, G. et al., "Deterministic BIST with Multiple Scan Chains", Proceedings of the International Test Conference, 1998, pp. 1057 - 1064, International Test Conference, Washington, D.C., USA.	
PC	10	KRISHNA, C.V. et al., "Reducing Test Data Volume Using LFSR Reseeding with Seed Compression", Proceedings of the International Test Conference, 2002, pp. 321 - 330, International Test Conference, Washington, D.C., USA.	
PC	11	McCLUSKEY, E. J., "Test Data Compression", Design & Test of Computers, March - April 2003, pp. 76 - 87, Volume 20, Issue 2, IEEE Computer Society and the IEEE Circuits and Systems Society, USA.	
PC	12	RAJSKI, J. et al., "Embedded Deterministic Test for Low Cost Manufacturing Test", Proceedings of the International Test Conference, 2002, pp. 310 - 310, International Test Conference, Washington, D. C., USA.	

Examiner Signature	/Phung Chung/	Date Considered	01/17/2007
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